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DIRECT DIGITAL SYNTHESIZER IN A NEW MATHEMATICAL BASIS

Polikarovskykh O.I.

O. S. Popov Odessa National Academy of Telecommunications,
1 Kuznechna St., Odessa, 65029, Ukraine.
polalexey@gmail.com

ЦИФРОВИЙ СИНТЕЗАТОР ПРЯМОГО СИНТЕЗУ У НОВОМУ МАТЕМАТИЧНОМУ БАЗИСІ

Полікаровських О.І.

Одеська національна академія зв'язку ім. О.С. Попова,
65029, Україна, м. Одеса, вул. Кузнечна, 1.
polalexey@gmail.com

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Поликаровских А.И.

Одесская национальная академия связи им. А.С. Попова,
65029, Украина, г. Одесса, ул. Кузнечная, 1.
polalexey@gmail.com

Abstract. The principles of the construction and operation of a digital synthesizer for direct frequency synthesis with acceleration of computational operations by using a residual class system (RNS) are considered. The specifics of the implementation of the operation of direct and inverse transformations from the positional number system to the number system of the residual classes are described. A mathematical model of a synthesizer with a phase accumulator in the system of residual classes is considered. The ways of designing a digital synthesizer of direct synthesis with a phase accumulator in the RNS system and a sinusoidal DAC are considered. In traditional schemes, the conversion of residuals to the value of an analog signal occurs in several stages, where conversion to a binary system is one of the stages. This procedure degrades the speed of the RNS system, adding additional constraints and increasing the waiting time for the conversion result. Methods of converting from RNS to binary number system for basic operations are considered. A DDS design with a phase accumulator in the residual class system and a converter to an analog signal form without using a slow ROM is proposed. The problems of efficient use of the synthesizer crystal area and reduction of delays in the formation of the output signal are considered. A study of one of the main functional blocks of a direct digital frequency synthesizer, a digital-to-analog converter, has been carried out. The architecture of a direct digital frequency synthesizer with a DAC direct conversion from a non-positional number system to an analog signal is proposed. The main sources of noise generation in digital computational synthesizers of the proposed type are investigated. A mathematical model is proposed for calculating the power spectral density of phase noise, which will allow analyzing the noise characteristics in synthesizers built on the indicated principles.

Key words: RNS, Adder, DDS, CORDIC.

Анотація. Розглянуто принципи побудови та функціонування цифрового синтезатора прямого синтезу частоти з прискоренням обчислювальних операцій шляхом застосування системи залишкових класів (RNS). Описано специфіку реалізації операції прямого та зворотного перетворень із позиційної системи числення у систему числення залишкових класів. Розглянуто математичну модель синтезатора з фазовим акумулятором у системі залишкових класів. Розглянуто шляхи проектування цифрового синтезатора прямого синтезу з фазовим акумулятором у системі RNS та синусного типу ЦАП. У традиційних схемах перетворення залишків в значення аналогового сигналу

відбувається в кілька етапів, де перетворення в двійкову систему є одним із етапів. Ця процедура погіршує швидкість роботи системи RNS, додаючи додаткові обмеження та збільшуючи час очікування результату перетворення. Розглянуто методи перетворення з RNS у двійкову систему числення для основних операцій. Запропоновано конструкцію DDS з фазовим акумулятором у системі залишкових класів та перетворювачем в аналогову форму сигналу без використання повільного ПЗУ. Розглянуто проблеми ефективного використання площі кристала синтезатора та зменшення затримок при формуванні вихідного сигналу. Проведено дослідження одного з основних функціональних блоків прямого цифрового синтезатора частоти − цифро-аналогового перетворювача. Запропоновано архітектуру прямого цифрового синтезатора частоти з ЦАП безпосереднього перетворенням з непозиційної системи числення в аналоговий сигнал. Досліджено основні джерела виникнення шумів у цифрових обчислювальних синтезаторах пропонованого типу. Запропоновано математичну модель для обчислення спектральної густини потужності фазових шумів, що дасть можливість аналізувати шумові характеристики у синтезаторах побудованих на вказаних принципах.

Ключові слова: RNS, Adder, DDS, CORDIC.

Аннотация. Рассмотрены принципы построения и функционирования цифрового синтезатора прямого синтеза частоты с ускорением вычислительных операций путем применения системы остаточных классов (RNS). Описана специфика реализации операции прямого и обратного преобразований с позиционной системы счисления в систему счисления остаточных классов. Рассмотрена математическая модель синтезатора с фазовым аккумулятором в системе остаточных классов. Рассмотрены пути проектирования цифрового синтезатора прямого синтеза с фазовым аккумулятором в системе RNS и синусного типа ЦАП. В традиционных схемах преобразования остатков в значение аналогового сигнала происходит в несколько этапов, где преобразования в двоичную систему является одним из этапов. Эта процедура ухудшает скорость работы системы RNS, добавляя дополнительные ограничения и увеличивая время ожидания результата преобразования. Рассмотрены методы преобразования с RNS в двоичную систему счисления для основных операций. Предложена конструкция DDS с фазовым аккумулятором в системе остаточных классов и преобразователем в аналоговую форму сигнала без использования медленного ПЗУ. Рассмотрены проблемы эффективного использования площади кристалла синтезатора и уменьшение задержек при формировании выходного сигнала. Проведено исследование одного из основных функциональных блоков прямого цифрового синтезатора частоты - цифро-аналогового преобразователя. Предложена архитектура прямого цифрового синтезатора частоты с ЦАП непосредственного преобразованием с непозиционной системы счисления в аналоговый сигнал. Исследованы основные источники возникновения шумов в цифровых вычислительных синтезаторах предлагаемого типа. Предложена математическая модель для вычисления спектральной плотности мощности фазовых шумов, что позволит анализировать шумовые характеристики в синтезаторах построенных на указанных прнципа.

Ключевые слова: RNS, Adder, DDS, CORDIC.

A key role of direct digital synthesis arising in digital systems of frequency synthesis and signals is the speed of processing the values of samples of synthesized signals, the speed of data processing and, in turn, the energy efficiency of such systems. Accuracy and speed, determined by the need for many of calculations in the process of digital applications, have a significant effect on the quality of synthesized signals. The main ways to solve these problems is the modernization of digital synthesis systems by using more efficient methods of calculation [1,2,3,4,5].

Considering the requirements for building high-performance computing devices, including those applicable in digital frequency and signal synthesis systems, the main method for solving the problem of increasing the speed of digital data being processed is confirmed, namely, a method that allows building the structure of a computing device of such a system with the maximum parallelization of performing arithmetic operations. This method in turn solves a number of tasks that are put before the computing device:

– Introduction of efficient algorithmic and hardware structures of parallel type.

– Ensuring a high degree of integration and unification of the arithmetic unit.

– Application of advanced error control.

– Use of variants of computer arithmetic, which are best suited for high-speed implementations of computational processes that require large amounts of computation [6,7,8].

Problem statement. The use of a conventional system of binary numbers in arithmetic operations on large amounts of data causes a number of difficulties caused by the presence of inter-bit connections. This disadvantage imposes limitations on the ways of implementing arithmetic operations, thereby complicating the hardware and limiting the system's performance. Therefore, it is expedient to use such arithmetic, in which the bitwise relations in the calculations were absent or were minimized. The arithmetic possessing the specified properties is the non-positioning system of numbering - the system of residual classes (RNS). Thus, the search for ways to solve the problem of increasing productivity led to the idea of independent parallel processing of data and, consequently, the replacement of the usual binary system with the system of residual classes.

In this system, their remainders represent the numbers from dividing by the chosen base system, and all rational operations can be performed parallel to the digits of each digit separately. However, a system of residual classes that is so convenient in one respect is inherent in a number of shortcomings in other respects: the limited effect of this system on the field of positive integers, the difficulty in determining the ratio of numbers in terms of value, determining the outcome of an operation from a range, etc. In turn, these shortcomings require effective ways to overcome them [9].

In the RNS the numbers are represented in the basis of prime mutually numbers which called modules $\beta = \{p_1,...p_k\}$, $GCD(p_i, p_j) = 1$ where $i \neq j$. The product $P = \sum_{i=1}^{k} p_i$ of all modules RNS is called - dynamic range of the system. Any integer number in the range $0 \le X \le P$ can be uniquely represented in the RNS as the vector $\{x_1, x_2,...., x_k\}$, there $x_i = |X|_{p_i} = X \bmod p_i$ [2]. Dynamic range of RNS is usually divided into two approximately equal parts, so that approximately half of the dynamic range represented positive numbers, and the rest of the dynamic range - negative. Suchthat any integer satisfies one of the following two relations:

$$\begin{aligned} -\frac{P-1}{2} \le X \le \frac{P-1}{2}, \text{ for odd } P, \\ -\frac{P}{2} \le X \le \frac{P}{2}, \text{ for even } P, \end{aligned} \tag{1}$$

may be presented in the RNS.

The operations of subtraction, addition and multiplication in a RNS are represented by formulas:

$$\begin{aligned} A \pm B &= (\alpha_1, \alpha_2,..\alpha_n) \pm (\beta_1, \beta_2,..\beta_n) = \\ &= ((\alpha_1 \pm \beta_1) \bmod p_1, (\alpha_2 \pm \beta_2) \bmod p_2,.... \\ &..,(\alpha_n \pm \beta_n) \bmod p_n; \end{aligned} \tag{2}$$

$$\begin{aligned} A \times B &= (\alpha_1, \alpha_2,..\alpha_n) \times (\beta_1, \beta_2,..\beta_n) = \\ &= ((\alpha_1 \times \beta_1) \bmod p_1, (\alpha_2 \times \beta_2) \bmod p_2,.... \\ &..,(\alpha_n \times \beta_n) \bmod p_n; \end{aligned} \tag{3}$$

Equations (2) - (3) show the parallel nature of the RNS, free from bit transfers. These operations are called modular, since for their processing it is necessary to operate with small numbers (residues) arising as a result of division into a set of modules, and for obtaining numerical values only one clock cycle is required [10]. To convert numbers from the binary position number system to RNS we use an algorithm based on the application of a distributed arithmetic. K-bit number X is divided into separate formats, for each of which is assigned a pre-known number of B-binary discharges. Then the n-bit binary number can be expressed as a combination $\frac{n}{B}$ - positional formats with the

dimension B bits. This position of each format is assigned a specific weight 2^j , where $j = 0, B, 2B, ..., MB$

$$X = \sum_{j=0}^{M} (\sum_{i=0}^{B-1} x_i 2^i) 2^j ,$$

where B - number of digits of the selected format; M - the degree of the format; x_i - a factor of 0 or 1; $j = 0, B, 2B, ..., MB$ is the position of the format; i - the position of the digit in the format. Convert a number from binary position code into the modular code is carried out using a modular summation of the remainders modulo m_i:

$$X = \left| \sum_{j=0}^{M} (\left| \sum_{i=0}^{B-1} x_i 2^i \right|_{m_i}) 2^j \right|_{m_i} .$$

Restoring the number X by the remainders $\{x_1, x_2, ..., x_k\}$ is based on the Chinese residue theorem

$$X = \left| \sum_{i=0}^{k} \left| P_i^{-1} \right|_{p_i} P_i \right|_p \tag{4}$$

where $P_i = \frac{P}{p_i}$. Element $\left| P_i^{-1} \right|_{p_i}$ means a multiplicative inverse for P_i, by module p_i [2].

The advantages of representing numbers in RNS can be represented as follows:

1. Since there is no propagation of transfer between arithmetic blocks in the RNS, and numbers of large dimension are represented as small residues, this leads to acceleration in the processing of data.
2. When presenting data using RNS, a large number of numbers are encoded in a set of small numbers of residues, and, accordingly, the complexity of computing devices in each channel modules is reduced, which facilitates and simplifies the operation of the computer system.
3. The RNS is a non-positioning system without the lack of dependence between its arithmetic blocks; therefore, an error in one channel does not extend to others, which in turn facilitates the process of detecting and correcting errors.

Thus, the use of RNS makes it possible to simplify and reduce the architecture of electronic computing devices, thereby increasing not only the speed, but also the energy efficiency of products.

However, operations such as comparison of two numbers, division and the detection of a sign are laborious and expensive in RNS. Many solutions have been proposed for these problematic operations. Most of them consist in converting the remainder into a binary system (the inverse transformation). On the other hand, choosing the right set of modules is another important issue for building an effective RNS with a sufficient dynamic range.

Results and analysis. Summing up some results, it can be noted that the system of residual classes allows significant improvement in the parameters of a computer in a Direct Digital Synthesizers (DDS) in comparison with a computer built on the same physical and technological basis, but in a positional system calculation, and to receive new more progressive constructive and structural solutions.

The essence of digital frequency synthesis is the conversion of the digital code of the number A into an analog harmonic signal with a frequency

$$f_{out} = \frac{F_{CLK} \cdot A}{M},\ 0 \le A \le M, \tag{5}$$

where F_{CLK} - frequency of the clock generator; M is a fixed positive integer, based on the application of the periodicity property of a harmonic function analogous to the property of arithmetic operations modulo the ring of integers.

In the proposed device, the formation of a harmonic oscillation $X(t) = U\cos(2\pi f_{out} t)$ is carried out by obtaining its samples at times $t = \Delta t \cdot k$ with the clock frequency $F_{CLK} = 1/\Delta t$.

Taking into account (5), the discrete samples of a harmonic oscillation with amplitude U are described by the expression:

$$\begin{aligned} X(\Delta t \cdot k) &= U \cdot \cos(2\pi f_{out} \cdot \Delta t \cdot k) = \\ &= U \cdot \cos(2\pi F_T \cdot \frac{A}{M} \cdot \Delta t \cdot k) = \\ &= U \cdot \cos(\frac{2\pi A k}{M}), \end{aligned} \tag{6}$$

where $k = \overline{0, \infty}$. Since the cosine is a periodic function then

$$\frac{2\pi k}{M} \bmod 2\pi = \frac{2\pi}{M}(k) \bmod M.$$

Therefore, k can be formed within the period $k = \overline{0, M-1}$. An arbitrary nonnegative integer A can be represented in the code of the residual number system. The integer A in the range $0 \le A \le \prod_{i=1}^{N} m_i$ is uniquely coded by its residues a_i on the bases m_i:

$$A = (a_1, a_2, ..., a_N),$$

there

$$a_i = A - \left[\frac{A}{m_i}\right] \cdot m_i = (A) \bmod m_i$$

$[\ ]$ - the integer part of number; $m_1, m_2, ..., m_N$ - a set of relatively prime positive integers, called bases; N - number of bases.

The code in the RNS of the result of the product C of the numbers A and k is determined by computing the individual products of the residues for each base:

$$\begin{aligned} A \cdot k = C[k] &= (c_1[k], ..., c_N[k]) = \\ &= ((a_1 \cdot \chi_1) \bmod m_1, ..., (a_N \cdot \chi_N) \bmod m_N)' \end{aligned}$$

where $c_i[k] = (a_i \cdot \chi_i) \bmod m_i$, $i = \overline{1, N}$.

We represent (6) in the form

$$X(\Delta t \cdot k) = U \cdot \cos(\frac{2\pi}{M} \cdot C[k]) = \\ = U \cdot \cos(\frac{2\pi}{M} \cdot C[k]) \bmod M. \quad (7)$$

A discrete samples, directly proportional to the (7) can be formed in the agile modular adder [11].

Fig.1 shows a block diagram of a high-speed direct digital frequency synthesizer with a flexible architecture.

The Phase Accumulator (shown below in Fig.1) performs modulo M addition where $m_1 = 2^{P+2}$ for non-negative p. It consists of n finite state machines (FSM) performing phase accumulation modulo m_i. In [11] recommends the use of a finite state machine in place of modulo adder for the phase accumulator since the delay can be of only two logic levels. The input to finite state machine is the binary encoded i-th residue digit $|k|_{m_i}$ of the frequency setting word. The state of finite state machines in the time is the binary encoded i-th residue digit of the phase at that time.

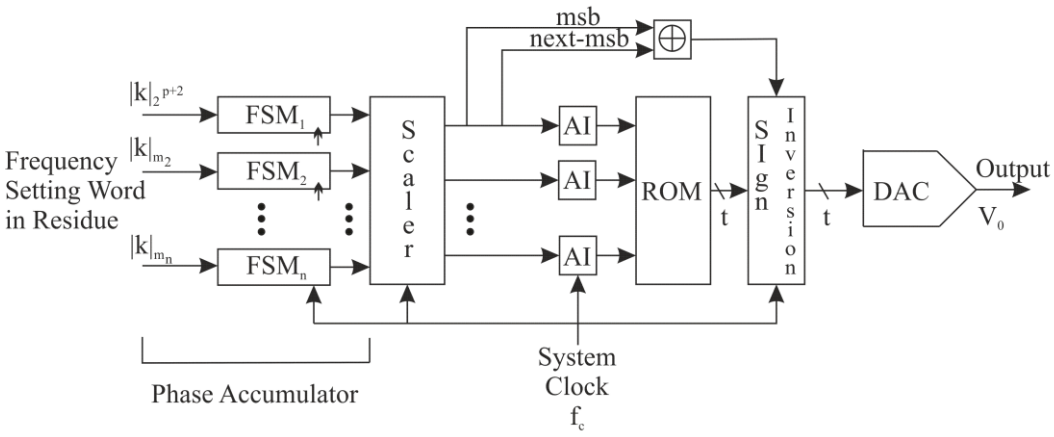

Figure 1 – Frequency Agile Direct Synthesizer [11]

The values of the phase words entering the DAC can be calculated based on the CRT (Chinese residue theorem) on the remnants. The inverting unit of the phase-word address (AI) in Fig. 1 performs an additional inverting by modulus m_i so that it can achieve the symmetry of the output harmonic signal.

However, the author of work [9] has convincingly proved that in such a structural scheme the use of a permanent storage device with values of the sine function is impossible.

The correct solution is to save the results of the transformation of the harmonic CRT function into the ROM, where the value of the residues remains. Accordingly, inverting blocks (AI), the value of the higher bit in the architecture of the high-speed direct digital frequency synthesizer in Fig. 1 are also not useful because of the lack of symmetry information. It is clear that in the proposed structural scheme of the synthesizer the size of the permanent memory device will increase significantly. Thus, the increase in speed, as can be seen from the analysis of the synthesizer, occurs in the phase accumulator, which has a smaller length of the phase word than binary systems, and the scaling of the harmonic function actually introduces additional operations, reducing the speed of the synthesis of signals, respectively, makes it possible to reduce the required volume of ROM. However, it should be noted that a ROM that corresponds to a certain balance uses as the address all bits of a word. Inversion blocks and exclusive blocks OR for older and

subsequent bits are also not required [12].

In addition to the classical DDS structure, there are a number of methods for converting the values of the phase accumulator into a harmonic waveform. The existing methods have been analyzed; the results of this analysis of the most common methods are given in Table 1.

These methods can be implemented in the RNS system, separately the method of Taylor series approximation [13, 14] and the CORDIC algorithm [15, 16, 17, 18] can be singled out. In these methods, multipliers are used whose implementation in the RNS system is much more efficient than in the binary system. In [19] an even simpler method for synthesizing a harmonic signal of a given frequency from the values of the phase accumulator was proposed. The most effective approach in terms of reducing the crystal area of a synthesizer of direct digital synthesis is the use of blocks of amplitude-phase conversion without the use of a ROM.

Table 1 − Comparative table of different methods of phase-amplitude transformation with a resampling level of -85 dB

Method	**Memory capacity**	**Coefficient of compression**	**Additional required chips**	**Retraction achieved in model**	**Note**
Classic method	$2^{14} \times 12$ bit	1:1	-	-97,23 dB	-
Sunderland Architecture	$2^8 \times 9$ bit $2^8 \times 4$ bit	59:1	Adder	-86,91 dB	Simple implementation
Nikola's architecture	$2^8 \times 9$ bit $2^8 \times 4$ bit	59:1	Adder	-86,81 dB	Simple implementation
Approximation in Taylor series with two additions	$2^7 \times 9$ bit $2^7 \times 5$ bit	110:1	Adder multiplier	-85,88 dB	The need for a multiplier
Algorithm CORDIC	-	-	14 states, 18 bit – length of internal transformation	-84,25 dB	Great computational complexity

In Fig. 2 the functional diagram of the proposed direct digital frequency synthesizer without a ROM is presented. DDS replaces the ROM and the linear DAC on a sine-weighted digital-to-analog converter that serves as a phase-amplitude conversion unit and at the same time, it is a DAC. This solution leads to the fact that there is no need for a ROM, which is a relatively low speed and bottleneck for DDS high-speed. An important issue to be solved in such a synthesizer scheme is the construction of a sinus-weighted DAC with a nonlinear distribution of segments in the phase-amplitude converter.

The ways of designing a digital phase-frequency synthesizer with a phase accumulator in the system of RNS and sinus-weighted type of DAC were considered. In traditional schemes, the conversion of the remainder to analog occurs in several stages, where the conversion to a binary system is one of the stages. This procedure worsens the speed of the whole RNS system by adding additional constraints and increasing the waiting time for the conversion result. Therefore, a direct remainder to analog converter is sought to solve that problem and make the RNS efficient. The problem of direct transition from the rest to the analogue is not yet sufficiently worked out in modern works. In [19], the author proposed his direction of solving the problem, namely, a direct analog converter, based on a mixed radix system.

The main disadvantage of the converter based on the mixed radix system is the sequential algorithm of work, which makes it for a large dynamic range of frequencies slow to the use of a combination of a phase accumulator built in the system of residual classes to a digital-to-analog converter with a direct transformation into a harmonic signal based on the Chinese CRT is

proposed. Such a converter eliminates the need for an intermediate stage of conversion into a binary system of calculation and can be much more productive than the direct converted residue-to-binary system. Consequently, the need for a large area modular adder disappears. Instead, the summing operational amplifier is used to perform a modular addition in the analog form. The proposed converter facilitates the realization of CRT in the need for direct conversion into analog form and is suitable for systems with a wide dynamic range.

CRT is not a sequential algorithm, as opposed to the mixed radix system. The value of each balance can be generated simultaneously using the ROM search tables. Consequently, the proposed architecture for direct conversion from RNS to an analog form is presented in Fig.3.

The synthesizer consists of the following functional blocks: the binary code converter into the RNS system, the phase accumulator in the RNS, the RNS processor, the conversion units based on the CRT, the DAC units and the summing operational amplifier. The frequency control word (FCW) is fed to the binary code converter in the residual class system. In the phase accumulator, the phase values are accumulated for each of the residues in the RNS system. In the RNS processor, the necessary transformations of signals - phase transformation, amplitudes, modulation of the synthesized oscillation - occur. After this, the received signal in the form of its values in the RNS enters separately into conversion units based on the CRT system. The resulting values are converted into an analog form in the DAC units [19].

To find the necessary balance to the analog converter in the phase accumulator, partial sums are added. The algorithm works based on permanent storage devices of small size. The volume of the ROM for partial sums will be $(2^k \times 3k)$ -bit ROM in the case where the size of the residue is a k bit.

The value of each partial amount is converted into an analog form by a separate digital-to-analog converter. In the future, the final addition of analogue values of partial sums in a single analogue adder based on the add-amplifier is carried out.

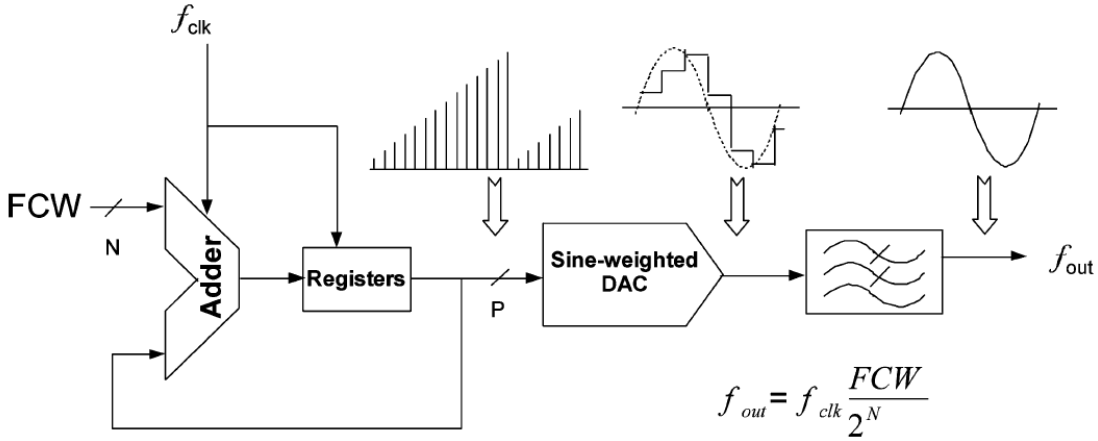

Figure 2 – Structural scheme of the ROM-free DDS [19]

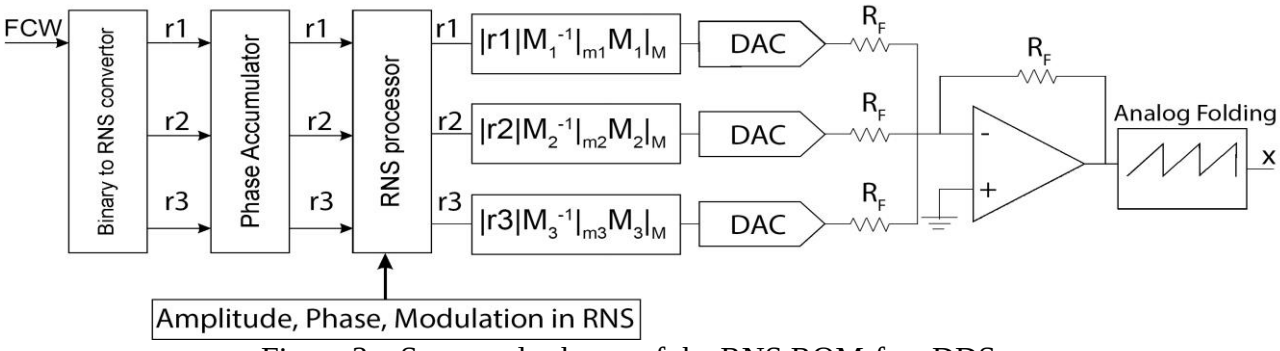

Figure 3 – Structural scheme of the RNS ROM-free DDS

The delay in the complete conversion of the synthesized signal is

$$t_{all} = t_{rom} + t_{DAC} + t_{summer}. \quad (8)$$

For large residual values - *k*, the size of the ROM begins to increase and at a certain stage becomes a bottleneck for increasing the speed of DDS. The ROM area is of critical importance for the construction of high-speed DDS. The proposed DDS will consume power comparable to the converter described in [20].

RNS DDS with a traditional R / B converter and DAC will be less effective than the proposed structure due to the significant loss of speed of the residue to binary number system converter. The speed of work proposed by us RNS ROM-free DDS will be roughly higher in proportion to the number of partial DACs (see Fig. 3). However, the increase in the number of DACs leads to increased distortions of the synthesized signal.

In the RNS ROM-free DDS synthesizer, the output form of the DDS signal will be distorted from phase and amplitude distortion due to a small number of quantization levels in the DACs. In addition, there will be side effects of components in the spectrum of the output signal that are inherent to all DDS synthesizers. The form of distribution of the components of the output spectrum of the DDS signal can be found by the corresponding analytical expression

$$f_E = f_{clk} \cdot \frac{2^{N-1} \bmod(2^{N-1}-1)}{2^{N-1}} = f_{clk} \cdot \left(\frac{1}{2}\right)^{N-1},$$

where *N* is the bit length of the main frequency word before transformation into a system of residual classes. The phase noise models of the proposed synthesizer were analyzed. From the analysis, it can be concluded that the spectral density of phase noise power RNS DDS can be represented as a sum of three components: the spectral density of phase noise of the clock generator, quantization noise and own noise of the synthesizer elements:

$$S_{outDDS}(F) = S_T(F)K_{DDS}^2 + S_{qn}(F) + S_{own}(F),$$

where $K_{DDS}^2 = (f_{out} / f_T)^2$ – the coefficient of transmission of DDS by noise; f_T and f_{out} - the clock and output frequencies; F – the frequency offset from the carrier. The phase noise analysis of RNS DDS has shown that they have additional deviations (up to 5 dB/Hz) compared with the experimental noise characteristics of modern integral DDS.

Conclusion. A direct digital synthesizer (DDS) with phase accumulator and residue-to-analog converter based on the Chinese residue theorem was proposed. A new structural scheme of RNS DDS without transforming into a binary representation form was proposed. The proposed RNS DAC implements the Chinese theorem on the remnants with the help of analog circuit elements and is most suitable for the implementation of the DDS.

The proposed remainder to analog converter was compared to the MRC based remainder to analog converter, and to the CRT based R/B converter. The key features of the proposed remainder to analog converter are:

1. The proposed solution made it possible not to use large modular aggregates, which occupy a large area on the crystal. Instead, it uses rather simple manufacturing and designing amplifiers.

2. The proposed architecture reduces the size of the ROM, which is a very important factor in the design direct digital synthesizers for fast switching.

3. The structure of a perspective synthesizer of direct digital synthesis is analyzed. The values of the potential SFDR and methods for its improvement are analyzed.

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