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DIRECT DIGITAL FREQUENCY SYNTHESIZER BASED ON FIBONACCI CODES

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ПРЯМІ ЦИФРОВІ СИНТЕЗАТОРИ ЧАСТОТИ НА ОСНОВІ КОДІВ ФІБОНАЧЧІ

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Abstract. A principle of construction of the direct digital frequency synthesizers and their place in the modern synthesis radio systems was proposed. The proposed structure of the phase synthesizer accumulators based on Fibonacci codes that will increase the bit synths and improve their frequency response range expansion in the direction of the synthesized signals. We consider a method of Fibonacci DAC will create precision DDS.

Анотація. Розглянуто принципи побудови прямих цифрових синтезаторів частоти та їх місце у сучасних системах синтезу радіосигналів. Запропоновані структури синтезаторів із фазовими акумуляторами на основі кодів Фібоначчі, що дасть можливість збільшити розрядність синтезаторів, покращити їх частотні характеристики у бік розширення діапазону синтезованих сигналів. Запропоновано у якості вихідного ЦАП прямого цифрового синтезатора частоти використовувати ЦАП у кодах Фібоначчі, що дозволить створити синтезатори із високою точністю.

Direct digital frequency synthesizer plays an important role in modern electronic devices. This is achieved by many significant advantages: speed reconfiguration frequency, high distinguished ability, wide bandwidth synthesized Multi DDS owing to, manufacturability, reliability, miniaturization capabilities and unique technical characteristics (phase continuity when switching from frequency to frequency, signal the possibility of forming complex shapes, digitally controlled amplitude, frequency and phase of the output fluctuation) is currently been used in communication systems. Especially promising is the use of DDS in radio transmission systems with high noise immunity of information and security. One of the limiting factors for maximum speed and quality spectral composition of synthesizers is the speed of some arithmetic operations in the core of the digital synthesizer [1].

For example, if we add two binary numbers

$$011111111 + 000000001 = 1000000000 \ ,$$

that while there is a "long hyphen" from LSB, which is the principal factor that reduces the maximum synthesized frequency synthesizer. Attempts to overcome these disadvantages binary system led to the creation of numerous number systems with a wide range of properties:

- The system of residual classes;
- A system with an integrated manner;
- Negative positional numeral system;
- Factorial notation;
- Binomial number system and others.

All these number systems have certain advantages in comparison with the binary system and were aimed at overcoming the lack of reporting and improve the performance of the adder as a basic element of any computer system. The greatest popularity of ternary number system [2] and the system of residual classes [3], on which achieved set purpose computer processors and special applications.

In this paper Stakhov A.P. [4] describes approaches to the construction of a new coding theory based on Fibonacci numbers. Consider the use of a new coding theory to construct high-speed direct digital frequency synthesizer (DDS).

The paper necessary to consider the theoretical foundations of Use Fibonacci representation codes for building high- accumulative adder, which is the phase accumulator DDS It is necessary to analyze its

performance. It is necessary to consider the principles of DAC codes in Fibonacci, and its application to build DDS with improved tactical and technical characteristics. Make a comparison of the proposed synthesizer Fibonacci existing classic direct digital synthesis.

To implement DDS of Fibonacci codes, consider a block diagram of a classical synthesizer which is presented in Figure 1. The structure consists of the following functional blocks: phase accumulator, which is a classic accumulative adder; Permanent memory - phase- amplitude converter, DAC, digital-to- analog converter and output filter HF
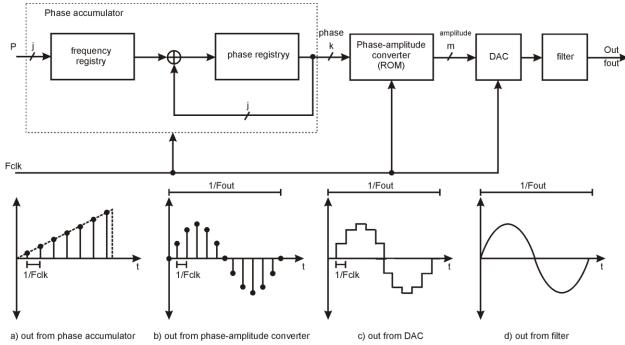

Figure 1 – Block diagram DDS and signal conversion rates.

Consider replacing the accumulator on the accumulator phases from phase meter adder and Fibonacci codes Fibonacci counter. Based on the convolution operation and scanning have significant advantages compared to binary counters. Counting units in the Fibonacci code (summarizing counter) is as follows. Before adding items to LSB level output representation that corresponds to the number is converted to a form that the value of the LSB was 0. Then added to 1 LSB, which leads to the fact that the numerical value of the counter becomes equal then Fibonacci representation of the number is given in the following form to LSB value was equal to 0. Demonstrate this:

$$
\begin{aligned}
&000000+1=000001=000010=1\\
&000010+1=000011=000100=2\\
&000100+1=000101=000110=3\\
&000110+1=001001=001010=4\\
&001010+1=001011=001100=5\\
&001100+1=010001=010010=6\\
&010010+1=010011=010100=7\\
&010100+1=010101=010110=8\\
&010110+1=011001=100010=9\\
&100010+1=100011=100100=10\\
&\ldots\\
&101010+1=101011=000000=0.
\end{aligned}
\tag{1}
$$

Fibonacci counting system is that in any situation of transition among N to $N+1$, performed during the follow-up to two convolutions. The last line of (1) is a Fibonacci overflow counter. Convolution operation is called basic arithmetic Fibonacci, based on four basic micro-operations [5]:

Convolution: $011 \rightarrow 100$ **Deconvolution:** $100 \rightarrow 011$

$$\text{Moving:} \downarrow = \begin{matrix} 1 & 0 \\ 0 & 1 \end{matrix} \qquad \text{Absorption:} \downarrow = \begin{matrix} 1 & 0 \\ 1 & 0 \end{matrix}$$

Convolution operation and scanning based on the main recurrence relation (2). These operations are one-that is executed as part of a combination Fibonacci, located in the same case. Micro-transactions and acquisitions are double, that is performed as part of the combination, which is located in two registers.

$$F(n) = F(n-1) + F(n-2); F(0) = 0, F(1) = 1, \tag{2}$$

there $n \in \{0, \pm 1, \pm 2, \pm 3, ...\}$.

The algorithm operation Adder meter shows that such meters laid the foundations of designing high-speed counters without using complicated schemes of group transfer.

However, to build DDS more important is its use as a accumulator meter and the phase is not accumulative adder. Consider as an example the addition of these Fibonacci number:

$$A_0 = 010100100 \text{ i } B_0 = 001010100.$$

In addition Fibonacci we use micro-transactions moving, rolls and sweep. The amount formed in lowercase B.

The first step consists of performing all possible displacements binary 1 from registry A to B:

$$A_0 = 010100100$$
$$\downarrow \downarrow$$
$$\underline{B_0 = 001010100}.$$
$$A_1 = 010100100$$
$$B_1 = 010100100$$

The second step consists of the execution of all possible binary combinations of reaming and all possible combinations of convolutions in binary B_1, namely

$$A_1 = 000000100 \rightarrow A_2 = 000000011$$
$$B_1 = 011110100 \rightarrow B_2 = 100110100.$$

The third step is to perform all possible displacements binary 1 in case A in registry B:

$$A_2 = 000000011$$
$$\downarrow \downarrow$$
$$\underline{B_2 = 100110100}$$
$$A_3 = 000000000$$
$$B_3 = 100110111$$

Adding completed because all binary 1 moved from register A to register B. After bringing Fibonacci binary combinations B_3 to minimal form, we get the sum $B_3 = A + B$ presented in minimal form:

$$B_3 = 100110111 = 101001001 = 101001010.$$

So adding two digit numbers many possible three cycles of the input frequency, regardless of the input bit codeword.

In addition to the phase accumulator important role, and perhaps decisive, in DDS played DAC output quality by parameters provides power spectral density of the amplitude and phase noise synthesized signal source. In order not to carry out the conversion phase value at the output of the phase accumulator in point binary representation can be used as a DAC is not a classic device, and Fibonacci DAC [6].

DAC in Figure 1 converts Fibonacci 5-bit code into electric voltage U_{out} at the DAC output. The number of bits DAC can be extended to any n by expanding Fibonacci resistive divider from left to right. Fibonacci DAC contains n (on fig.1. n =5) standard generators of electric current I_0 in n electric switch $K_0 - K_n$. Will be the switch guided binary digits $a_n..a_2a_1a_0$ golden code p - proportion. Based on which, established way positional representation of numbers:

$$A = a_i \Phi_p^i \tag{3}$$

where $a_i \in \{0,1\}$ - binary digit i -th, $i = 0, \pm 1, \pm 2, \pm 3, ...$, Φ_p - radix.

For the case $a_i = 1$ switch $K_i (i = 0,1,2,3,...,n)$ is in the closed position, $a_i = 0$ switched off. It can be shown that the closed switch K_i leads to the appearance of the next voltage at the point of i:

$$U_i = \beta_p I_0 R \tag{4}$$

where $\beta_p = 1/(1 + \Phi_p^{-1})$. Voltage (4) is transferred from i -th point to $i+1$ -th point of the transmission coefficient $1/\Phi_p$, while at the DAC output voltage occurs next:

$$U_{out} = \frac{\beta_p I_0 R}{\Phi_p^{n-i-1}} = \frac{\beta_p I_0 R}{\Phi_p^{n-1} \times \Phi_p^{-1}} = \frac{\beta_p I_0 R}{\Phi_p^{n-1}} \times \Phi_p^i \tag{5}$$
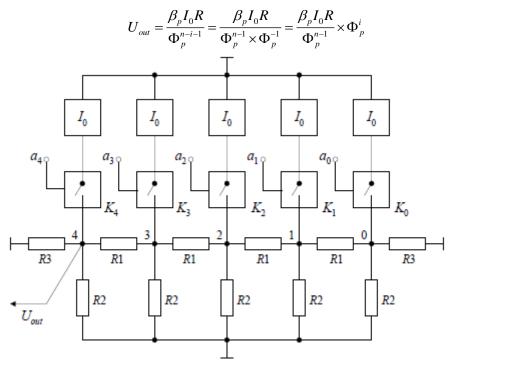

Figure 2 – Digital-to-Analog Converter Fibonacci

Using the principle of superposition it is easily to calculate the output voltage of the DAC when applied to the input of DAC n - bit code golden ratio $a_{n-1}a_{n-2}..a_2a_1a_0$:

$$U_{out} = B_{p}\sum_{i=0}^{n-1} a_i \Phi_p^i \tag{6}$$

where $B_p = \dfrac{\beta_p I_0 R}{\Phi_p^{n-1}}$. As the (6) DAC in Figure 2, converts the code "golden" proportions $a_{n-1}a_{n-2}...a_2a_1a_0$ in the equivalent electrical voltage U_{out} up to a constant factor B_p.

This allows you to control the DAC linearity in the production and operation [6]. This property DAC Fibonacci makes it very perspective for use in systems DDS.

CONCLUSIONS

In this paper we analyze the prospective direct digital frequency synthesizer based on Fibonacci codes

The analysis of the structural elements of the synthesizer, especially switch elements: phase accumulator and digital-to- analog converter. It is shown that DDS based on Fibonacci codes will have some significant advantages of classic DDS: no the problem of delay in the transfer phase accumulator - the result of the phase accumulator will always appear at the third step of the reference oscillator; possibility of building codes in the DAC Fibonacci.

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